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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/159,569	09/24/1998	RYOJI SUZUKI	P98.1699	5302

7590 10/06/2003

DAVID R METZGER ESQ
SONNENSCHEIN NATH & ROSENTHAL
P O BOX #061080
WACKER DRIVE STATION SEARS TOWER
CHICAGO, IL 60606

EXAMINER	
WHIPKEY, JASON T	

ART UNIT	PAPER NUMBER
2612	14

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/159,569	SUZUKI ET AL.	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 19, 2003, has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 14, and 16 have been considered but are moot in view of the new ground of rejection.

Drawings

3. The replacement drawing sheet was received on May 19, 2003. This drawing is approved.

Claim Objections

4. The cancellation of claim 8 obviates the objection to the claims. No claim objections remain.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 3-6, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer (U.S. Patent No. 5,973,311) in view of Yamazaki (U.S. Patent No. 5,818,070).

Regarding claim 1, Sauer shows in Figure 4 a two-dimensional matrix of pixels. Each pixel, as shown in Figure 2, has a photodetector P11, such as a photodiode, to integrate photo-generated charge (column 5, lines 13-15). The pixel also includes a selection switch TR11 and a read-out switch TC11. Both switches read out the charge stored in photodetector 11 to a signal line (column 5, lines 24-27).

Though buffer 38 is shown to be connected to signal line 72 in Figure 4, an amplifier may also be used (column 6, lines 30-33). A separate buffer/amplifier is connected to signal line 74. The buffer/amplifier outputs an electrical signal to output signal line 30 (column 5, line 62 through column 6, line 2). Signal lines 46 and 74 have reset switches 64 and 66, respectively, for resetting the lines (column 7, lines 50-54).

Sauer is silent with regard to using a double-gated transistor in his pixels.

Yamazaki shows in figures 4B and 4C a structure that can form an image sensor (column 1, lines 33-34; column 13, lines 19-20). A dual gate (see title) CMOS circuit (column 6, line 24) includes gate electrodes 103 and 113 (column 6, line 40; column 7, lines 17-18), which are connected to first and second gate electrodes 102 and 112 (column 8, lines 35-42). First and second gate electrodes 102 and 112 "are formed so that they substantially overlap each other" (column 2, lines 14-16).

An advantage to constructing double-gate transistors with overlapping electrodes is that the size of the image sensor may be reduced. For this reason, it would have

been obvious at the time of invention to have Sauer combine the two transistors in each pixel into a single double-gate transistor with overlapping electrodes.

Regarding claims 3 and 4, Sauer teaches that the signal lines are reset before readout from the pixels begins (column 7, lines 61-64).

Regarding claim 5, Sauer shows in Figure 2 that two switches TC11 and TR11 are connected in series between photodetector P11 and the signal line.

Regarding claim 6, Sauer shows in Figure 2 that selection switch TR11 is on the side of the photodetector P11.

As for claim 11, Sauer teaches that switches 40 and 44 are provided between signal lines 72 and 74, respectively, and output line 30. Since switch 40, for example, is turned on by row select line 26 and resetting of the signal line 46 is performed when charges are not being output to it (column 7, lines 61-64), resetting of signal line 46 must occur when switch 40 is off. Therefore, switch 40 allows signal line 46 to reach a reset level during a reset time by not connecting the line to output signal line 40. Additionally, switch 49 must output the signal from buffer/amplifier 38 to output signal line 40 in order for the system to be useful.

Regarding claims 12 and 13, Sauer teaches that a correlated double sampling circuit may be included (column 13, lines 50-52).

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer in view of Yamazaki and further in view of Gowda (U.S. Patent No. 5,898,168).

Claim 2 may be treated like claim 1. However, both Sauer and Yamazaki are silent with regard to using a hole accumulation diode sensor structure.

Gowda discloses a pixel circuit for an image sensor. A photodiode 26 is shown in Figure 3B. Photodiode 26 may be a pinned photodiode (column 7, lines 9-10). Official Notice is taken that a pinned photodiode is the same as a hole accumulation diode. As described in column 7, lines 18-21, the advantage of using a pinned photodiode is that it does not need to be reset after each read. For this reason, it would have been obvious for Sauer to include a pinned photodiode, such as the one described by Gowda.

9. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer in view of Yamazaki and further in view of Munier (4,609,824).

Claim 9 may be treated like claim 1. However, both Sauer and Yamazaki are silent with regard to connecting the read-out switch between the photodetector and the signal line and connecting the selection switch to a control electrode of the read-out switch and a read-out pulse line.

Munier shows an image sensor in Figure 2 with read-out transistor $T_{1,12}$ connected between photodiode D_{12} and electrode S_2. Selection transistor $T_{2,12}$ is connected to the control electrode of transistor $T_{1,12}$ and address line Y_3.

An advantage to this transistor configuration is that random pixel access is possible. For this reason, it would have been obvious for Sauer's pixel matrix to utilize the transistor configuration taught by Munier.

Regarding claim 10, Sauer, Yamazaki, and Munier are silent with regard to using a depression MOS transistor as the selection switch.

Official Notice is taken that depression-type MOSFETs require a lower voltage across the source and drain. Therefore, the advantage to using a depression-type MOSFET is that it has reduced power requirements. For this reason, it would have been obvious to have Munier's selection switch use a depression-type MOSFET.

10. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer in view of Yamazaki and further in view of Koch (U.S. Patent No. 4,628,364).

Regarding claim 14, Sauer shows in Figure 4 a two-dimensional matrix of pixels. Each pixel, shown in Figure 2, has a photodetector P11, such as a photodiode, to integrate photo-generated charge (column 5, lines 13-15). The pixel also includes a selection switch TR11 and a read-out switch TC11. Both switches read out the charge stored in photodetector 11 to a signal line (column 5, lines 24-27). A correlated double sampling circuit may also be included in the system (column 13, lines 50-52).

Sauer is silent with regard to using a double-gated transistor in his pixels.

Yamazaki shows in figures 4B and 4C a structure that can form an image sensor (column 1, lines 33-34; column 13, lines 19-20). A dual gate (see title) CMOS circuit (column 6, line 24) includes gate electrodes 103 and 113 (column 6, line 40; column 7, lines 17-18), which are connected to first and second gate electrodes 102 and 112 (column 8, lines 35-42). First and second gate electrodes 102 and 112 "are formed so that they substantially overlap each other" (column 2, lines 14-16).

An advantage to constructing double-gate transistors with overlapping electrodes is that the size of the image sensor may be reduced. For this reason, it would have been obvious at the time of invention to have Sauer combine the two transistors in each pixel into a single double-gate transistor with overlapping electrodes.

Sauer is also silent with regard to outputting a reset level followed by a signal level and calculating the difference between the two.

Koch discloses a two-dimensional image sensor (Figure 1) with a pixel configuration similar to Sauer's. Koch's sensor performs correlated double sampling. In a reset state, the output of the pixels in the first sensor column, for example, is placed on line SP1, which is connected to horizontal line AL by transistor ST1 (column 5, lines 34-45). This reset signal is processed by the CDS circuitry shown in Figure 3. Actual sensor signals, including noise, are output similarly using the same circuitry (column 5, lines 49-55). The CDS circuitry then calculates the difference between the two signals to output a "clean" image signal (column 5, lines 55-58).

An advantage to performing correlated double sampling using common circuitry for transferring both reset and signal outputs is that less circuitry is needed in the pixel area of the sensor while improving image quality. For this reason, it would have been obvious at the time of invention to have Sauer's sensor use shared circuitry to perform correlated double sampling, such as that described by Koch.

Regarding claim 15, Sauer discloses that output signal line 1 and output signal line 2, which are adjacent, may be enabled simultaneously (column 9, lines 11-12).

Two pixels on the same output signal line may also be enabled simultaneously (column 9, lines 1-4). This process is shown in Figure 7.

Claim 16 may be treated like claim 14. However, Sauer is silent with regard to using an optical system.

Official Notice is taken that optical systems are commonly associated with image sensors. The advantage to using an optical system with an imager is that images from a distance may be captured with great detail. For this reason, it would have been obvious to have Sauer's pixel matrix include an optical system.

Regarding claim 17, Sauer discloses that output signal line 1 and output signal line 2, which are adjacent, may be enabled simultaneously (column 9, lines 11-12). Two pixels on the same output signal line may also be enabled simultaneously (column 9, lines 1-4). This process is shown in Figure 7.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 9 A.M. to 6:30 P.M. eastern daylight time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communication and (703) 872-9315 for After Final communication.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 306-0377.

Response to this action should be mailed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to the appropriate number above for communications intended for entry. (For informal or draft communications, please label **"PROPOSED"** or **"DRAFT"**.) Hand-delivered responses should be brought to the sixth floor receptionist of Crystal Park II, 2121 Crystal Drive in Arlington, Virginia.

JTW
JTW
September 30, 2003

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600